**No. 2022-1906**

# UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VLSI TECHNOLOGY LLC,

*Plaintiff-Appellee*,

*v.*

INTEL CORPORATION,

*Defendant-Appellant.*

On Appeal from the United States District Court for the Western District of Texas in Case No. 6:21-cv-00057-ADA, Judge Alan D. Albright

## REPLY BRIEF FOR DEFENDANT-APPELLANT INTEL CORPORATION

AMANDA L. MAJOR
STEVEN J. HORN
WILMER CUTLER PICKERING
HALE AND DORR LLP
1875 Pennsylvania Avenue, NW
Washington, DC 20006
(202) 663-6000

MARY V. SOOTER
WILMER CUTLER PICKERING
HALE AND DORR LLP
1225 17th Street, Suite 2600
Denver, CO 80202
(720) 274-3135

WILLIAM F. LEE
JOSEPH J. MUELLER
LAUREN B. FLETCHER
BENJAMIN N. ERNST
ALISON BURTON
WILMER CUTLER PICKERING
HALE AND DORR LLP
60 State Street
Boston, MA 02109
(617) 526-6000
William.Lee@wilmerhale.com

*Attorneys for Defendant-Appellant Intel Corporation*

January 4, 2023

# CERTIFICATE OF INTEREST

Counsel for Defendant-Appellant Intel Corporation certifies the following:

**1. Represented Entities**. Fed. Cir. R. 47.4(a)(1). Provide the full names of all entities represented by undersigned counsel in this case.

Intel Corporation.

**2. Real Party in Interest**. Fed. Cir. R. 47.4(a)(2). Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.

None.

**3. Parent Corporations and Stockholders**. Fed. Cir. R. 47.4(a)(3). Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.

None.

**4. Legal Representatives**. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

WILMER CUTLER PICKERING HALE AND DORR LLP: Arthur W. Coviello, Jeffrey A. Dennhardt, Felicia H. Ellsworth, Jordan L. Hirsch, Thomas Lampert, Gregory H. Lantier, James M. Lyons, George F. Manley, Alexis Pfeiffer, Kate Saxton, Joshua L. Stern, Louis W. Tompros, Anh-Khoa Tran, Paul T. Vanderslice

KELLY HART & HALLMAN LLP: J. Stephen Ravel, Kelly Ransom, Sven Stricker (former)

PILLSBURY WINTHROP SHAW PITTMAN LLP: Brian C. Nash (former)

KIRKLAND & ELLIS LLP: John C. O'Quinn

James Eric Wren, III

**5. Related Cases**. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). *See also* Fed. Cir. R. 47.5(b).

*VLSI Technology LLC v. Intel Corp.*, No. 6:21-cv-00299-ADA (W.D. Tex.) (formerly No. 6:19-cv-00255-ADA);

*VLSI Technology LLC v. Intel Corp.*, No. 6:19-cv-00977-ADA (W.D. Tex.) (formerly No. 6:19-cv-256-ADA);

*VLSI Technology LLC v. Intel Corp.*, No. 1:18-cv-966-CFC (D. Del.);

*VLSI Technology LLC v. Intel Corp.*, No. 5:17-cv-05671-BLF (N.D. Cal.);

*Intel Corp. v. Fortress Investment Group*, No. 2021-0021-MTZ (Del. Ch.);

*OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2021-01064 (PTAB);

*Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2021-01229 (PTAB);

*Intel Corp. v. VLSI Technology LLC*, IPR2022-00366 (PTAB) (joined with IPR2021-01064);

*Intel Corp. v. VLSI Technology LLC*, IPR2022-00479 (PTAB) (joined with IPR2021-01229).

**6. Organizational Victims and Bankruptcy Cases**. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

None.

Dated: January 4, 2023

/s/ William F. Lee
WILLIAM F. LEE
WILMER CUTLER PICKERING
HALE AND DORR LLP
60 State Street
Boston, MA 02109
(617) 526-6000

# TABLE OF CONTENTS

# TABLE OF AUTHORITIES

## CASES

Page(s)

**STATUTES AND RULES**

## OTHER AUTHORITIES

## INTRODUCTION

VLSI attempts to defend the infringement verdicts by doubling down on its expert's hand-waving analysis—relying on Dr. Conte's unsupported conclusions, his infringement theories that were contrary to the claim language and prosecution history, and even his expert report which was not before the jury. Meanwhile, VLSI ignores Dr. Conte's critical trial admissions and brushes aside the Intel documents describing how the accused features were actually implemented in Intel's products. VLSI also repeatedly tries to shift the burden to Intel, though it was VLSI's burden to prove infringement. Despite its bluster, VLSI identifies no substantial evidence of infringement for either patent. The judgment should be reversed.

As for damages, VLSI's response confirms that it convinced the jury and the district court to endorse—in Fortress's words—an "oversized award[]" based on the "sheer complexity" of Intel's products and damages evidence not tied to "specific patent claim[s]."[1] VLSI admits, for example, that it presented large numbers to the jury through ***noncomparable*** settlement agreements. It tries—and fails—to justify that brazen violation of this Court's precedent by rewriting the district court's rulings, blaming Intel for presenting a damages defense, and implausibly denying that Intel was prejudiced. Regarding its damages model, VLSI concedes that its

[1] Zur, *Why Investment-Friendly Patents Spell Trouble for Trolls* (Sept. 24, 2015), https://knowledge.wharton.upenn.edu/article/why-investment-friendly-patents-spell-trouble-for-trolls/.

economic and technical experts relied on ***non-accused*** products and features in their calculations and told the jury about Intel's ***total accused revenues***. VLSI's purported excuses for these weighty errors fall far short of showing that its experts' testimony was reliable and admissible, but instead demonstrate that VLSI did not seek to value only the patented technology. At minimum, a new trial is required.

## ARGUMENT

### I. THE '373 PATENT INFRINGEMENT JUDGMENT SHOULD BE REVERSED.

#### A. VLSI Fails To Identify Substantial Evidence For The "When" Limitations.

VLSI feigns ignorance as to how the claims require ***using*** a memory's "minimum operating voltage" in determining "when" to supply either of two voltages to the memory (Br. 34), but the claim language is clear. It specifies which voltage to provide depending on whether a first regulated voltage is above or below the "minimum operating voltage":

| Condition | Voltage Provided To The Memory |
|---|---|
| "when the first regulated voltage is ***at least the minimum operating voltage***" | "first regulated voltage" |
| "when the first regulated voltage is ***below the minimum operating voltage***" | "second regulated voltage" |

Appx111(14:8-13); *see id.*(13:20-27).[2] Indeed, the patent's whole point is to use the memory's "minimum operating voltage" for this purpose. Appx101 (abstract: "This

[2] Emphasis added unless indicated otherwise.

***minimum operating voltage*** information can then be ***used in determining when*** an alternative power supply voltage may be switched to the memory[.]").

As at trial, VLSI identifies no evidence that Intel's products use RING_RETENTION_VOLTAGE (the alleged "minimum operating voltage") in determining "when" to provide VCCR (the alleged "first regulated voltage") or VCCIO (the alleged "second regulated voltage") to the C6SRAM (the alleged "memory"). In fact, VLSI acknowledges that Intel's products switch the C6SRAM's power supply from VCCR to VCCIO "[w]hen" the chip enters the Package-C7 state. Br. 32. That has nothing to do with RING_RETENTION_VOLTAGE—as Dr. Conte admitted in testimony VLSI fails to address (Appx2735-2736)—and therefore cannot literally satisfy the claims. Intel Br. 33-36.[3]

Because the accused voltage-switching functionality is triggered by the Package-C7 state rather than anything relating to an alleged "minimum operating voltage," Intel's products do not follow the "when" limitations' conditions. For example, VCCR is provided to the C6SRAM at times when it is ***less than*** RING_RETENTION_VOLTAGE—the ***opposite*** of the claims. Intel Br. 35. VLSI's only response is to insist that VCCR can ***never*** drop below

[3] VLSI nowhere defends the district court's statement that "RING_RETENTION_VOLTAGE acts as the ***threshold*** for when the voltages are supplied." Appx80-81. That is undisputedly not how Intel's products work.

RING_RETENTION_VOLTAGE during active modes. Br. 31-32. But Intel's fuse data—which VLSI ignores—shows that VCCR does operate below RING_RETENTION_VOLTAGE for certain active modes. *Infra* pp. 5-9.

VLSI's assertion that VCCIO is supplied when VCCR is eventually "reduced" to zero (Br. 32-33) also cannot prove infringement. When the chip enters Package-C7, a multiplexer ***first*** switches the C6SRAM's supply from VCCR to VCCIO and ***then*** reduces VCCR's voltage. Appx1862-1863. While VLSI notes VCCR "is 'slowly ramp[ed] down' before being turned off" (Br. 33 (alteration original)), Dr. Conte admitted the "ramp[ing] down" occurs "when the mu[ltiplexer] is ***already switched***" to VCCIO. Appx2673. Thus, at least when the chip first enters Package-C7, VCCIO is supplied to the C6SRAM when VCCR is still ***at or above*** RING_RETENTION_VOLTAGE. *See* VLSI Br. 32 (admitting VCCR only "falls below RING_RETENTION_VOLTAGE as it is gradually reduced to zero"). Again, that is ***opposite*** the "when" limitations.

VLSI alleges "[o]ther Intel documents confirm" Dr. Conte's opinion. Br. 33. Yet VLSI cites only an Intel specification confirming that Intel's multiplexer switches when the chip enters Package-C7. Appx8830-8831 (multiplexer switches when "Vccr is powered down"). Moreover, VLSI ignores Intel's source code, which definitively shows that RING_RETENTION_VOLTAGE plays no role in the accused voltage-switching functionality. Intel Br. 34-36.

Nor is this a matter of claim construction. VLSI Br. 34. Intel's noninfringement defense applies the claims' plain meaning. It is also consistent with the patent specification, including the "controller" embodiments. Appx107(5:41-53) (controller indicates which supply to select, including by "determining when" a first voltage (VDDlogic) is below a "minimum" operating voltage); Appx108(8:16-47) (similar). VLSI's infringement theory, by contrast, treats the "when" limitations as though they do not reference the memory's "minimum operating voltage" at all. The verdict cannot be sustained on that basis. *Wisconsin Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1348 (Fed. Cir. 2018) (reversing infringement verdict premised on Dr. Conte's testimony, noting that plain meaning "does not leave the term devoid of any meaning").

### B. VLSI Fails To Identify Substantial Evidence For The "Minimum Operating Voltage" Limitations.

As Intel explained, RING_RETENTION_VOLTAGE cannot literally be a "***minimum*** operating voltage" of the C6SRAM because Intel's products are "fully operational" at a ***lower*** voltage. Intel Br. 26-33. VLSI's scattershot response fails to identify substantial evidence supporting the verdict.

1. VLSI points to two Intel documents describing RING_RETENTION_VOLTAGE as a "worst case retention voltage," but concedes these documents refer to a retention voltage for ***the entire RING domain*** rather than the C6SRAM alone. Br. 24-25 (citing Appx9574; Appx12642). VLSI treats this as

good enough because Dr. Conte testified that "all the memory" in the RING is built from the same circuitry. Appx2424. But VLSI had to prove RING_RETENTION_VOLTAGE is a minimum operating voltage of the C6SRAM specifically (the accused "memory" (Appx1403)), not of "all the memory" in the RING. And as Intel's expert explained, this difference matters because the C6SRAM is only a small fraction of the RING's memory. Appx1950-1953; Appx15344-15346. Remarkably, in arguing "[t]he jury reasonably credited Conte's testimony," VLSI cites his ***expert report***—which was not before the jury and cannot support the verdict. Br. 25 (citing Appx3236, Appx3267).

VLSI claims "other Intel documents further confirm Conte's testimony," but the only document it cites is Dr. Conte's unadmitted report again. Br. 25 (citing Appx3235). VLSI also references testimony from Intel's expert, but that testimony confirmed he did ***not*** "find anything in Intel documents on minimum operating voltage for C6 SRAM." Appx1986. If VLSI meant to refer to the Intel spreadsheet discussed in Intel's opening brief (Br. 31 (citing Appx11359-11362)), Intel's expert—the ***only*** witness who testified about that document—explained that its "Vmin" was unrelated to RING_RETENTION_VOLTAGE or any "minimum operating voltage." Appx2013-2015; *see* Appx1985-1989.

2. VLSI's response to the ***specific voltages implemented in Intel's products*** fares no better. The fuse data collected from Intel's products shows they

are "fully operational" at a RING_VF_VOLTAGE_0 voltage (0.6719 or 0.6172 volts) ***"significantly lower"*** than RING_RETENTION_VOLTAGE (0.7617 or 0.7500 volts). Intel Br. 27-30.[4] VLSI does not deny these voltage values are fused into Intel's products or identify any other specific voltages used—though Dr. Conte presumably could have done so were there different voltages to identify.

VLSI instead contends that Intel's expert should have adjusted the voltages to compensate for different temperatures. Br. 25-27. But VLSI relies only on Dr. Conte's unsupported assertions and identifies no substantial evidence indicating that the fused voltage values are not actually used in the products or that temperature compensation must always (if ever) be done. *See* Appx2425-2431. Rather, Intel's engineer explained that the RING_VF_VOLTAGE_0 voltage is "one of the voltages that would be used," even recognizing that temperature affects "which voltage level is set[.]" Appx2758-2759; *see* Appx14252-14280 (source code engineer discussed). And Dr. Conte admitted that the RING_VF_VOLTAGE_0 described by this engineer "[i]s a ***voltage*** that's actually used[.]" Appx2436-2437. VLSI nowhere addresses this testimony.

[4] While VLSI denigrates Intel's demonstratives (Br. 26-27), they illustrate technical information directly from Intel's fuse data and source code. Appx1850-1860; Appx2757-2760; Appx1945-1950; Appx2015-2017; Appx2742-2744; Appx14232-14251 (fuse-data analysis); Appx14252-14280 (source code).

Nor does VLSI identify substantial evidence supporting Dr. Conte's assertion that RING_VF_VOLTAGE_0 is "***always*** above" RING_RETENTION_VOLTAGE "[w]hen you compensate for temperature[.]" Br. 28-29 (quoting Appx2430). VLSI cites a graph that says nothing about RING_RETENTION_VOLTAGE, the specific fuse values or voltages implemented in Intel's products, or temperature compensation. Appx19243[5]; Appx2017. And in response to Dr. Conte's admission that the document containing this graph was "not a final description of the products" (Intel Br. 31 (quoting Appx2435-2436)), VLSI merely says Intel "never identified a different version[.]" Br. 29. But it was not Intel's burden to ensure that VLSI's expert relied on documents reflecting the voltages actually used in Intel's products. Even so, Intel did identify the fuse data—which does exactly that.

3. In a last-ditch attempt to defend the verdict, VLSI suggests it was not actually required to prove that RING_RETENTION_VOLTAGE "is ***literally*** the '***minimum*** retention voltage' for the C6SRAM[.]" Br. 29 (emphases original). Of course it was. That was VLSI's only infringement theory. Appx1451; Appx2731.

VLSI also blames Intel for not seeking a construction of "minimum operating voltage." Br. 29-30. But there was no need for any construction, as the parties agreed to apply plain meaning. Appx2532. There was likewise no dispute about

[5] Intel cited this page as Appx14103. This document nowhere mentions "Vmin" as VLSI mistakenly suggests. Br. 29.

what that plain meaning was: Dr. Conte testified that "minimum operating voltage," as used in the claims, means "you['ve] got to keep power on the memory and ***you['ve] got to keep above this***" minimum voltage. Appx1403. He also agreed a "minimum retention voltage" is the ***"lowest"*** voltage at which the memory can reliably hold data. Appx2730-2731. Again, VLSI ignores this testimony.

Even if the patent potentially allows for different "minimum operating voltages" at different temperatures (VLSI Br. 30), VLSI never suggested at trial that was how Intel's products work. As VLSI acknowledges, Dr. Conte's only infringement theory was that "RING_RETENTION_VOLTAGE stores the ***minimum*** voltage at which memory—the C6SRAM—can retain data." Br. 24. Because the evidence does not support that theory adopted by the jury, the judgment should be reversed.

## II. THE '759 PATENT INFRINGEMENT JUDGMENT SHOULD BE REVERSED.

### A. VLSI Fails To Identify Substantial Evidence For The "Request" Limitations.

Each claim requires a "master device" that sends a "request" to change frequency and a "clock controller" that receives that request. Appx123-124(8:50-9:4, 9:19-40). The jury correctly rejected VLSI's literal-infringement theory, which alleged that Intel's processor core ***alone*** sends the request, and VLSI does not challenge that finding. Appx9. VLSI fails to identify substantial evidence supporting the jury's finding of infringement by equivalents, which adopted VLSI's

theory that the ***combination*** of Intel's core with p-code on the PCU provides the request and that the PCU ***also*** receives that request.

1. VLSI points to Dr. Conte's conclusory testimony on equivalents, but identifies no testimony explaining how the alleged equivalent provides the request in "substantially the same way" as claimed. Br. 37 (citing Appx2704-2709). All VLSI can muster is that Dr. Conte ***identified*** the alleged equivalent ("it's the first master device and its P-code that provides the request") and acknowledged it was ***different*** from the "master device" providing the request as claimed ("'[i]t's just a[]' … 'difference of where an engineer draws [a] data line'"). Br. 37 (citing Appx2707). But noting a "difference" between two things is a far cry from explaining how they operate in "substantially the same" way. Dr. Conte never "articulate[d] how the difference[]" was "insubstantial," and his "scant" testimony cannot support the verdict. *Akzo Nobel Coatings, Inc. v. Dow Chem. Co.*, 811 F.3d 1334, 1342-1343 (Fed. Cir. 2016).

VLSI tries to backfill Dr. Conte's deficient equivalents analysis by citing his literal-infringement testimony. Br. 36-37 (citing Appx2691-2692; Appx2697; Appx2699-2701). But unlike his equivalents theory, Dr. Conte's literal-infringement theory alleged that the core ***alone*** sends a "request" and identified a ***different*** signal (called "Core_Active") as the alleged "request." Appx2690-2692; Appx15153; Appx85. Such testimony "solicited for purposes of establishing literal

infringement … [i]s insufficient to establish infringement [by] equivalents." *Texas Instruments, Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1566-1568 (Fed. Cir. 1996).

VLSI's cited cases merely recognize that equivalents ***may*** apply where two accused elements perform a single claimed function. Br. 37-38. Moreover, unlike here, the patentees in VLSI's two cases where infringement was found presented testimony explaining how the alleged equivalent was "an insubstantial change in the way the element performed its function." *Hughes Aircraft Co. v. United States*, 140 F.3d 1470, 1475 (Fed. Cir. 1998), *abrogated by Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 234 F.3d 558 (Fed. Cir. 2000); *see Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991) ("There was testimony fully supporting the ALJ's findings[.]").

VLSI cannot avoid its burden to prove equivalents with "particularized testimony" by asserting that "Intel's expert never testified that it was technically significant that the P-code was located in the PCU." Br. 38; *see Akzo*, 811 F.3d at 1342. Nevertheless, Intel's witnesses did explain why this matters: because, unlike the cores, only the PCU can calculate speed changes (the alleged "request") using algorithms based on ***system-wide*** telemetry data. Appx2083-2085; Appx2146-2147; Appx2181-2184; Appx2196, Appx2762-2763; Appx15435-15437.

Nor can VLSI circumvent its proof requirements for equivalents by suggesting "the claim term 'master device' ***itself***" may include a core in combination with p-code. Br. 38 (emphasis original). That is not an infringement theory VLSI presented at trial. Instead, Dr. Conte contended the core/p-code combination infringed ***only*** by equivalents. Appx2707-2709; Appx15183.

2. Even setting aside the above problems with Dr. Conte's testimony, no reasonable jury could accept VLSI's nonsensical equivalents theory. As VLSI's own description confirms, the plain claim language recites two different elements: one that sends the request to change frequency, and another that receives that request. Br. 35 (explaining "master device" sends request, whereas "clock controller" receives request provided by master device). VLSI's contrived equivalents theory simply does not fit with that arrangement.

Rather, VLSI alleged that one of Intel's components (the PCU) involved in sending the request ***also*** receives the request. Intel Br. 43-44. Although VLSI now asserts that two "separate" components or modules inside the PCU perform those functions, all VLSI points to is code running on the PCU. Br. 38-39 (conceding what Dr. Conte called the "core['s] p-code" and "decision instructions" is all "physically located in the PCU"). Regardless, Dr. Conte undisputedly testified that the PCU—the component he alleged was the "clock controller"—provides and

receives the request. Appx2706-2707(54:23-25, 55:10-11); Appx2451(1451:12-16). That cannot be squared with the claim language.

### B. Prosecution History Estoppel Bars VLSI's Equivalents Theory.

To overcome repeated rejections, the applicant amended the claims to require that "the master device" provide the request to change frequency, rather than allowing the master device in combination with other components ("the at least one master device") to provide that request. Intel Br. 38-42. VLSI does not deny that, if these amendments narrowed claim scope, prosecution history estoppel bars its equivalents theory. Br. 39-44. VLSI's labored reading of the prosecution history fails to support its contention that there was no claim narrowing.

1. VLSI insists the "master device" amendments were "wholly unrelated to Ansari." Br. 40. Yet it cannot deny that: (1) the examiner repeatedly rejected the claims over Ansari (Appx8205; Appx8257; Appx8305-8306; Appx8349); (2) the applicant subsequently canceled and amended the claims, including by rewriting the "master device" limitations (Appx8316-8317; Appx8367-8368); and (3) the examiner thereafter withdrew the Ansari-based rejections (Appx8392-8394; Appx8432-8435; Appx8472). This sequence is "a highly influential piece of prosecution history" indicating the applicant narrowed the claims to overcome the Ansari-based rejections. *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1348 (Fed. Cir. 1998).

VLSI nonetheless asserts the "master device" amendments were not made to distinguish Ansari because "[t]he debate" between the applicant and examiner involved "the nature of the 'request,' not the component that sends the request" to change frequency. Br. 41-42 (emphases omitted). But the "debate" was not so narrow: the examiner's rejections and applicant's responses expressly discussed ***two of Ansari's components***—its "master device" and "arbiter"—in connection with the "at least one master device" limitations. Appx8205; Appx8257; Appx8305-8306; Appx8349; Appx8242-8243; Appx8277-8278; Appx8319; Appx8325. That makes sense because Ansari's "master device" generated a request relating to bus control (not frequency), whereas Ansari's "arbiter" determined which frequency to use. Appx4493(11:4-14); Appx4490(5:19-22); Appx8242-8243. Although VLSI now suggests Ansari's arbiter could not be involved in providing a request to change frequency because it ***also*** "receives the request" (Br. 42 (emphasis omitted)), that is exactly what VLSI alleged Intel's products do through equivalents. *Supra* pp. 12-13. Prosecution history estoppel bars VLSI from recapturing that surrendered claim scope.[6]

[6] VLSI's one-sentence waiver allegation is meritless. Br. 42. VLSI misstates Intel's argument (Intel Br. 38), which Intel made in its Rule 52 and 50 motions. Appx6892-6896; Appx6846-6852; Appx6868-6870; Appx4081.

Attempting to distract from this clear estoppel, VLSI points to ***additional*** prosecution arguments and amendments concerning the "characteristics" of the claimed request. Br. 41-42. But that cannot negate the estoppel arising from the "master device" limitations, including the amendments about which component(s) provide the request to change frequency. *Felix v. American Honda Motor Co.*, 562 F.3d 1167, 1182-1184 (Fed. Cir. 2009) (holding prosecution history estoppel "attaches to ***each*** added limitation").

2. VLSI alternatively suggests the "master device" amendments were made for "brevity and simplification" and "grammatical preference." Br. 40, 42-43. It identifies nothing in the prosecution history indicating that. Rather, VLSI's cited pages refer to the applicant's ***substantive*** arguments distinguishing Ansari. Appx8372-8373.

VLSI also speculates that the "master device" amendments "avoid[ed] the examiner objecting to grammatical 'informalities'[.]" Br. 44. But VLSI's lone prosecution history citation concerns the irrelevant "high frequency flag" limitations. Appx8196-8197. Regarding the "master device" limitations, Intel explained—and VLSI nowhere addresses—that the examiner's "informalities" comment referenced a ***later*** amendment fixing one claim. Intel Br. 42 n.11 (citing Appx8385; Appx8405). It did not undo the estoppel from the earlier narrowing amendments.

Finally, VLSI acknowledges that "a" and "the" should be interpreted in the singular when the context, including the prosecution history, "clearly evidences" such usage. Br. 43 (emphasis, alteration omitted). That is the case here: the narrowing amendments clearly demonstrate that "the master device" itself—not in combination with other components—must provide the claimed "request." Intel Br. 41-42. Prosecution history estoppel therefore bars VLSI's equivalents theory and requires reversal.

## III. THE DISTRICT COURT ERRONEOUSLY AND PREJUDICIALLY ALLOWED VLSI TO INTRODUCE *NONCOMPARABLE* AGREEMENTS.

VLSI acknowledges that the Intel settlement agreements it introduced were ***not comparable*** to the hypothetical negotiation and that noncomparable agreements are not a proper basis for calculating damages. Br. 44-49. Nevertheless, VLSI claims these agreements were admissible as "rebuttal." VLSI's arguments not only seek to rewrite what happened during and after trial, they cannot justify the erroneous admission of this prejudicial evidence.

1. The record belies VLSI's assertion that the noncomparable agreements "were not introduced to calculate damages." Br. 44. Consistent with his report disclosed long before trial, Mr. Chandler presented the noncomparable agreements as "informative" to the hypothetical negotiation used to determine a reasonable royalty and emphasized the "high-value amounts" paid by Intel. Appx2515-2516; Appx15231-15236; Appx6725-6730(¶¶162-166). Licenses, however, must be

"sufficiently comparable" to "***inform*** the hypothetical negotiation." *Elbit Sys. Land & C4I Ltd. v. Hughes Network Sys., LLC*, 927 F.3d 1292, 1299 (Fed. Cir. 2019). The district court abused its discretion by refusing to grant Intel's *Daubert* and pre-trial motions to exclude this evidence. Appx3570-3579; Appx3626-3629; Appx3723-3725.

2. Unable to defend its affirmative reliance on the noncomparable agreements, VLSI contends they were "proper rebuttal" because Intel told the jury that VLSI's damages demand was not "in the same universe" as what Intel pays for patent licenses in the "real world." Br. 44-46. VLSI omits, however, that Intel's statements were made in the context of discussing what Intel has paid in ***comparable*** agreements. Intel's opening statement referenced ***comparable*** agreements with Freescale and NXP. Appx1255 ("Freescale and NXP and Intel have entered into patent agreements.… [Y]ou'll see those licenses and the amount that's paid and you can decide which universe those licenses reside in."). Likewise, Intel's expert's testimony about the "real world," "going rate" for microprocessor patent licenses concerned twenty ***comparable*** Intel agreements. Appx2363-2366; Appx2764-2784; Appx15391-15409.

VLSI identifies no authority allowing noncomparable agreements as "rebuttal" to a comparable-license analysis, and this Court's precedent clearly forbids it. Intel Br. 46-51. Nor did VLSI offer the noncomparable agreements "to

rebut Intel's contention that there is 'some sort of a cap on the amount that Intel will pay,'" because Intel never suggested any such cap and VLSI cites only ***its own expert's*** testimony for that proposition. Br. 47 (citing Appx2803). Moreover, Intel's expert's testimony could not have been the basis for the district court's decision allowing the noncomparable agreements because Intel's expert testified ***after*** that ruling. Intel Br. 49 (citing Appx2328-2331). VLSI nowhere addresses this anomaly.

VLSI additionally contends that Intel's cross-examination of Dr. Sullivan regarding the purchase prices of various sports teams opened the door to the noncomparable agreements. Br. 45-47. That is also wrong. Contrary to VLSI's suggestion (Br. 48), the district court's admissibility ruling was ***not*** "clearly 'premised'" on this cross-examination. VLSI never argued during trial that Intel's cross-examination opened the door. Appx6831, Appx6835 (VLSI's responses to Intel's objections during trial). And when the court overruled Intel's objection to the noncomparable agreements, it simply remarked without explanation that it had "given Intel great liberty[.]" Appx2328. Even when VLSI raised its argument about Dr. Sullivan's cross-examination for the first time ***after*** trial (Appx6907-6908), the district court did not adopt it. The court instead stated it had admitted the noncomparable agreements as rebuttal to "Intel licenses" and "Intel's claimed licensing practices." Appx17-18. As discussed above, that was error. *Supra* pp. 16-18.

In any event, the noncomparable agreements would not have been proper rebuttal to Intel's cross-examination about sports-team prices. That cross-examination had nothing to do with Intel (or VLSI), patents, licenses, microprocessors, past Intel litigation, or the value of any licensed technology. It merely "put [Dr. Sullivan's] numbers in context" and impeached his credibility, including because Dr. Sullivan had previously described the $2 billion sale of one team as "astronomical." Appx1699-1701.

Even if Intel had opened the door at all (it did not), the district court never weighed "the extent to which otherwise inadmissible evidence is permitted" against "the unfair prejudice created." *Bearint ex rel. Bearint v. Dorell Juvenile Grp.*, 389 F.3d 1339, 1349 (11th Cir. 2004); *see Valadez v. Watkins Motor Lines, Inc.*, 758 F.3d 975, 981-982 (8th Cir. 2014) ("Otherwise, courts risk subverting … opening the door 'into a rule for injection of prejudice.'"). A new trial is required. *In re DePuy Orthopedics, Inc.*, 888 F.3d 753, 784-786 (5th Cir. 2018) (reversing decision allowing "recurring and 'highly prejudicial'" references to evidence leading to "colossal verdict" where defendants "supposedly 'opened the door'").[7]

[7] VLSI's cases are inapposite. Br. 46-47. In *Prism Technologies LLC v. Sprint Spectrum L.P.*, 849 F.3d 1360, 1371 (Fed. Cir. 2017), the patentee—unlike here—provided comparability evidence. *Silicon Graphics, Inc. v. ATI Technologies, Inc.*, 607 F.3d 784, 799 (Fed. Cir. 2010), did not involve noncomparable agreements.

3. VLSI's cry of no "unfair prejudice" to Intel lacks credibility given what happened at trial. VLSI repeatedly used the noncomparable agreements to skew the jury's damages horizon, suggest that Intel underpays for licenses absent litigation, and portray Intel as a serial infringer. Intel Br. 51-53. Although VLSI denies doing any of this (Br. 48-49), the trial record—and Mr. Chandler's demonstratives—tell a different story. Appx2501-2503; Appx2515-2516; Appx2620-2622; Appx2799-2806; Appx15231-15236.

VLSI further claims Intel was not prejudiced because the jury was instructed to consider whether an agreement is "sufficiently comparable." Br. 48. More fully, the instruction said: "whether [an] agreement is sufficiently comparable that it provides a reasonable indication of how the parties to the hypothetical negotiation would have negotiated a license[.]" Appx2549. While Mr. Chandler agreed the settlements were "noncomparable," he also testified that "the parties to the hypothetical negotiation would have found [them] informative[.]" Appx2515-2516. Regardless, no instruction could have avoided Intel's prejudice because the jury had already heard—several times—that Intel paid "hundreds of millions, if not billions" under the erroneously-admitted agreements. *E.g.*, *id.* And, in fact, the jury awarded amounts matching what Intel had paid under the two largest of those agreements. Intel Br. 53.

Because the jury's liability decision plainly "could … have been infected by" the noncomparable agreements, a new trial on liability and damages is warranted. Intel Br. 54. VLSI skips over Intel's cases reciting this standard. Br. 50.

## IV. VLSI'S DAMAGES MODEL SHOULD HAVE BEEN EXCLUDED AND CANNOT SUPPORT THE VERDICT.

Although VLSI "bears the burden of establishing the reliability of [its] expert's testimony," *Sims v. Kia Motors of Am., Inc.*, 839 F.3d 393, 400 (5th Cir. 2016), its explanations for Dr. Sullivan's damages model confirm that its experts' methodology was illogical and unreliable at every step. The district court abandoned its gatekeeping function when it allowed VLSI to present this made-for-litigation damages model to the jury. A new trial is required.

### A. Dr. Sullivan's Regression Was Not Tied To The Accused Products And Features.

VLSI does not dispute that Dr. Sullivan's regression ***included non-accused products*** and ***excluded the accused features***. *See* Intel Br. 55-59. VLSI's purported justifications for this approach do not withstand scrutiny.

1. VLSI contends Dr. Sullivan's regression used non-accused products to determine the price impact of speed across the "whole market." Br. 55-56. But that is precisely the problem. VLSI did not accuse the "whole market for Intel's processors" of infringement, and Dr. Sullivan never considered speed's impact on price in the accused products alone. VLSI's "fuel efficiency" analogy proves Intel's

point: just as it would make no sense to determine fuel efficiency's impact on the price of sportscars by looking at commuter cars, it makes no sense to value speed's impact on the price of the accused products by analyzing non-accused products.

VLSI's claim that Dr. Sullivan included non-accused products to make "comparison[s]" is equally illogical. Br. 56. There are hundreds of differences between the accused and non-accused products, and many non-accused features affect speed in all types of products. Appx5423(¶28); Appx5643-5645(Table 2); Appx1691. Dr. Sullivan's regression therefore could not have provided a meaningful comparison between products with and without the accused features with respect to speed's impact on price. *See* Appx3049(¶54); Appx3071(¶¶91-93). VLSI's citations do not show otherwise; they merely confirm Dr. Sullivan included non-accused products. Br. 55-56 (citing Appx3406(¶146); Appx3510-3511; Appx1620).

Dr. Sullivan's own math proves VLSI's "comparison" rationale is a facade. Dr. Sullivan considered the accused and non-accused products ***together*** in his dataset. Appx3406(¶146); Appx3510(178:19-179:5). He even calculated the ***same*** speed-to-price coefficient (0.764%) in his damages analyses for all eight patents asserted in Texas—though each involved ***different*** sets of accused products and features. Appx3471; Appx5959; Appx6110; Appx3044-3045(¶¶42-45). This one-

size-fits-all approach plainly did not quantify any speed-to-price relationship specific to the accused products here.

2. VLSI claims Dr. Sullivan excluded the accused features from his regression because he "analyzed how speed impacts price" and the accused features' benefits can be "translated" into "speed benefits." Br. 55 (emphases omitted). But by excluding the accused features, Dr. Sullivan ***ignored*** their contribution to speed in the speed-to-price coefficient he calculated. Moreover, many non-accused features undisputedly improve processor speed. Appx1691; Appx3499(117:2-119:22). Dr. Sullivan's speed-to-price coefficient was therefore impermissibly based on value attributable to non-accused features.

VLSI further asserts that Dr. Sullivan treated the non-accused features as "'control factors' to be excluded, leaving just the impact of speed on price." Br. 55 (emphases omitted). However, Dr. Sullivan's trial demonstrative shows he included over 35 non-accused features as ***"[p]rice [f]actors"*** in his regression. Appx15275. VLSI also ignores Dr. Sullivan's explanation that those non-accused features were "***included*** in [his] model" precisely because they were "potentially relevant to processor ***price***" and "informative." Appx3429(¶193); Appx3425(¶¶186-187).

VLSI notes that ***other*** steps in Dr. Sullivan's analysis purportedly addressed the accused products and features. Br. 55-56. Even if true, that cannot cure Dr. Sullivan's use of the wrong products and features in his regression, which led him

to use an erroneous speed-to-price coefficient in his damages calculations. "***[A]ny step*** that renders the [expert's] analysis unreliable" makes his testimony ***"inadmissible."*** *Moore v. Ashland Chem. Inc.*, 151 F.3d 269, 278 n.10 (5th Cir. 1998) (en banc).

3. VLSI urges that regression is "a powerful tool" and "commonly used." Br. 57. But the issue is not whether ***others*** have correctly used regression. It is whether ***Dr. Sullivan's*** regression—which included non-accused products and excluded the accused features—was sufficiently reliable to determine the "value attributable to the infringing features of the product, and no more." *Omega Patents, LLC v. CalAmp Corp.*, 13 F.4th 1361, 1376 (Fed. Cir. 2021). It was not, and VLSI identifies no authority supporting Dr. Sullivan's particular regression.

Far from endorsing Dr. Sullivan's methodology, the Federal Judicial Center's Reference Manual ("FJCRM") recognizes that "when inappropriately used" "regression analysis can confuse important issues while having little, if any, probative value." FJCRM at 308. That is the case here. The errors in Dr. Sullivan's regression mean he failed "to seek only those damages attributable to the infringing features." *VirnetX, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1326 (Fed. Cir. 2014).

**B. Dr. Sullivan Used Unreliable Technical Inputs.**

VLSI acknowledges that Dr. Sullivan's calculations used technical "inputs" derived from tests that included ***non-accused products and features***. Br. 57-59.

None of VLSI's excuses for these mistakes demonstrates that VLSI's experts reliably quantified the patented technology's benefits.

1. For the '373 patent, VLSI admits Dr. Annavaram relied on ***non-accused products*** and the ***non-accused Core-C7 state*** to select the Power Model "workload" for his calculations. Br. 57-58. VLSI nowhere explains how this approach calculated power savings for only the ***accused*** C6SRAM multiplexer feature.

VLSI instead accuses Intel of not challenging Dr. Annavaram's "analysis itself" or contending his "workload was unreliable." Br. 57-58. But that is exactly what Intel challenges: Dr. Annavaram relied on non-accused products and features to select a workload (Appx1555-1560) and used that incorrectly-selected workload as an "input" to the Power Model (Appx1533-1534), which he then used "to compute the power consumption" (Appx1530). Intel Br. 59-60. It does not matter that Dr. Annavaram's error occurred at an early step, as it still renders his whole analysis unreliable. *Moore*, 151 F.3d at 278 n.10.

VLSI also characterizes Dr. Annavaram's mistaken use of Core-C7 rather than Package-C7 data as "immaterial." Br. 58. But Dr. Annavaram's own analysis shows the "[r]esidency data"[8] he used to select the workload differed dramatically

[8] "[R]esidency" is "how often the chip resides in" a state. Appx1975.

between Core-C7 and Package-C7. Appx3132-3133(¶59) (Core-C7 ranges: 75-85%; Package-C7 ranges: 41-57%); Appx1578-1581; *see* Appx1975-1976. Although VLSI claims Dr. Annavaram's later "calculations" did not "include[] any CoreC7 data" (Br. 58), his workload selection was intended "[t]o approximate use of the [accused] C6 SRAM" and that is precisely where he used the incorrect Core-C7 data. Appx1558-1559; Appx1578-1581.

2. For the '759 patent, VLSI concedes Dr. Annavaram calculated power usage of ***the entire ring domain*** rather than just the ring bus/mesh. Br. 58-59. VLSI says this was "no mistake" because the ring domain and bus/mesh operate at the same ***frequency***. *Id.* That is beside the point. Dr. Annavaram was measuring ***power usage***, not frequency, and the entire ring domain necessarily draws more power than one of its components (the bus/mesh) alone. Appx5349-5350(¶¶696-699); Appx5372-5373(¶¶766-767); Appx2232-2234; Appx15488. That is why Dr. Conte instructed Dr. Annavaram to calculate only "the Ring ***bus's*** percentage of power drawn"—so they could, in Dr. Conte's words, "exclude the contribution of non-accused technologies, features, and functionalities[.]" Appx3215(¶1251). Dr. Annavaram's failure to follow that instruction resulted in a power-savings calculation not tailored to just the '759 patent's purported benefits.

### C. VLSI Improperly Sought Profit Disgorgement.

Dr. Sullivan also improperly allocated 100% of Intel's incremental profits to VLSI. Intel Br. 62-64. VLSI's responses fail to show that Dr. Sullivan's profit-split was either legally permissible or factually supported.

1. VLSI's waiver claim is meritless. Intel's *Daubert* motion expressly challenged Dr. Sullivan's "100-to-0 profit split in VLSI's favor." Appx3599 (emphasis omitted); *see* Appx3597-3600. While VLSI complains that Intel's motion did not use the word "disgorgement" (Br. 59), allocating 100% of incremental profits to the patentee is disgorgement and impermissible under 35 U.S.C. §284. VLSI never argues otherwise. Moreover, as VLSI acknowledges (Br. 59), Intel raised the issue again in its new-trial motion. Appx4106; Appx4962-4963.

2. VLSI contends there was no disgorgement because Dr. Sullivan's reduction of incremental revenues "does not reflect 'costs'" but instead provides "profit-sharing." Br. 60. Not so. Dr. Sullivan took the revenues Intel allegedly made from the patents-in-suit, reduced them by Intel's "total spending," and gave VLSI ***all*** resulting profits. Appx3461(¶296) (Dr. Sullivan explaining his 20-25% "cost apportionment and contribution apportionment" reduction as "deducting all total spending expenditures from net billings for the accused products"). Intel's "total spending" is its costs for the products; reducing product revenues by costs yields profits; and allocating that result to VLSI as damages is disgorgement.

VLSI also says Dr. Sullivan's profit-split was factually supported because he used Intel's "financial data." Br. 60-61 (citing Appx1662). But neither that assertion nor VLSI's lone citation to Dr. Sullivan's testimony shows his particular profit-split was "tied to" the hypothetical negotiation or "the facts of the case." *VirnetX*, 767 F.3d at 1334.

3. VLSI is wrong that the district court "was not required" to address Intel's profit-split arguments. Br. 61. In *United States v. Hodge*, 933 F.3d 468, 476-477 (5th Cir. 2019), the district court's "reasons for admitting" expert testimony were "stated in its [new-trial] order." By contrast, VLSI acknowledges this Court has remanded where the district court "failed to make ***any*** ruling" concerning the challenged testimony. Br. 61 (emphasis original) (citing *Finalrod IP, LLC v. John Crane, Inc.*, 838 F. App'x 562, 563 (Fed. Cir. 2021)). And here, the court ***never*** addressed Intel's profit-split arguments. Intel Br. 64.

**D. VLSI Violated The Entire Market Value Rule.**

VLSI asserts that Dr. Sullivan "mentioned" Intel's total accused revenues "only as a starting point to calculate damages[.]" Br. 62. But Dr. Sullivan did more than that: he told the jury that his calculated incremental revenues were only ***"a small piece, a sliver … of the overall revenues."*** Appx1655-1656; *see* Appx15290, Appx15292 (Dr. Sullivan's trial demonstratives showing incremental revenues next to total accused revenues). Although VLSI claims this testimony "was about

apportionment, not royalties" (Br. 62-63 (emphases omitted)), either way it was an attempt to justify Dr. Sullivan's damages numbers by comparison to Intel's overall accused revenues—which this Court forbids. *Uniloc USA, Inc. v. Microsoft Corp.*, 632 F.3d 1292, 1318-1321 (Fed. Cir. 2011). This also distinguishes *SynQor, Inc. v. Artesyn Technologies, Inc.*, 709 F.3d 1365, 1383 (Fed. Cir. 2013), because the patentee there "never sought to justify its damages figure" using "the price of the customer end products."

VLSI further says Dr. Sullivan "explain[ed] his calculation with numbers to avoid jury confusion." Br. 62. VLSI ignores, however, that Dr. Sullivan admitted he did ***not*** need to mention total accused revenues to explain his calculations. Intel Br. 65. The unfair prejudice of placing those large numbers before the jury therefore outweighed any probative value they could have.

## V. THE DISTRICT COURT ERRONEOUSLY DENIED INTEL'S MOTION TO AMEND.

VLSI attempts to rewrite the district court's opinion on Intel's license defense. Intel's argument that the license should be interpreted ***first*** in Delaware, in a suit involving all interested parties, did not waive Intel's right to present its license defense in this case. Appx3642-3643. Indeed, the district court treated Intel's request to sever and stay as a ***separate*** question mooted by its denial of leave to amend. Appx72. This Court cannot defer to reasoning the district court never

adopted, and the district court's actual reasons for denying leave to amend do not withstand scrutiny.

### A. Intel Timely Filed Its Motion And Preserved Its License Defense.

VLSI does not dispute that it was impossible for Intel to add a license defense before the scheduling order's deadline to amend. VLSI Br. 64. Nonetheless, analyzing Intel's motion under Rule 16(b)(4)—rather than Rule 15(a)—the district court purported to reject "Intel's explanation for a failure to timely comply with ***the scheduling order***." Appx67-68. To the extent the court was not relying on the scheduling order deadline, as VLSI now claims, it was addressing the wrong question. Appx67 (citing Rule 16 standard).

Moreover, the district court's discussion of the "three-month gap" before Intel filed its motion ignores critical context. Appx68. Fact discovery had closed, and the parties had served opening expert reports, before the Finjan acquisition. Appx5002. After the acquisition, Intel promptly notified VLSI of its license defense in August 2020. Appx3017-3019. But Intel was required to attempt to resolve the license dispute through a mandatory dispute-resolution process. Appx3694(§9.3). Although VLSI now claims that process did not apply to it, at the time VLSI

pointedly told Intel it refused to waive its rights under the process. Appx4502(46:13-47:7).[9]

Given the dispute-resolution process, Intel moved to stay in September 2020—before any other deadline passed—laying out the basis for its defense. Appx3001-3015. The district court never ruled on that motion. Meanwhile, gamesmanship delayed the dispute-resolution process. Intel requested mediation "as soon as possible," but Finjan delayed until December 2020. Appx5006; Appx5009. With the original trial date approaching, Intel had no choice but to preserve its rights in court. That does not mean the dispute-resolution process was optional. It shows Intel's diligence in the face of concerted delay.

Intel moved to amend less than three months after its initial letter and more than three months before trial began. The motion stated that "[t]o avoid any doubt that Intel has preserved its defense of license," Intel sought to add the defense. Appx3635. The motion also stated that Intel would sever and stay the defense to allow trial to proceed—a far cry from VLSI's claim that Intel sought to delay trial. Appx3640.

[9] The Chancery Court decision VLSI quotes addressed ***other*** infringement proceedings, admitted the court was "unclear" on the reasons for Intel's timing, did not consider the dispute-resolution process, and ***ruled that "Intel can and should pursue its license defense in the Infringement Actions."*** *Intel Corp. v. Fortress Investment Grp., LLC*, 2021 WL 4470091, at *7, *8 n.73 (Del. Ch. Sept. 30, 2021).

### B. Amendment Is Not Futile.

The district court's decision here directly conflicts with the ruling in the Delaware patent case that amendment to add Intel's license defense was not futile. Appx4498. VLSI's misreading of Delaware law and strained attempts to distance Fortress from VLSI do not meet the demanding standard for establishing futility.

VLSI acknowledges that courts applying Delaware law have bound non-signatory affiliates to a contract. Br. 68-69. VLSI's sole argument under Delaware law is that this rule applies only when "the non-party affiliate was under a signatory's control." Br. 68. That is incorrect. The relevant signatory to the agreement in *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, 213 A.3d 39 (Del. 2019), was CSH Theatres, but the Delaware Supreme Court held the agreement was binding on CSH's affiliates, including the family that controlled CSH and separate trusts and entities under the family's control. *Id.* at 42 & n.3, 44, 51, 56-58, 63.

VLSI also ignores that non-signatories can implicitly adopt a contract and its burdens by accepting the benefits of a contract made for a third party's benefit. *American Legacy Found. v. Lorillard Tobacco Co*., 831 A.2d 335, 349 (Del. Ch. 2003), *aff'd*, 903 A.2d 728, 745 (Del. 2006). Here, VLSI received the benefits of being brought under the License's definition of "Affiliates" (Intel Br. 71), but now seeks to disclaim the reciprocal burdens.

The Court should reject VLSI's strained efforts to avoid the License's plain language. The License's "Affiliates" definition depends on "control," not ownership. Appx3684(§1.2). Intel alleged common control by Fortress (Appx3674(¶154)), and quoted extensively from evidence showing control, including that Fortress employees hold a majority of VLSI's board seats (Appx3009-3010). The district court never examined whether Fortress exercised common control, instead resting its flawed analysis on Fortress not directly owning VLSI. Appx71.

Also incorrect is VLSI's argument—again, not adopted by the district court—that VLSI cannot license its patents without paying consideration to third parties. For example, VLSI could grant a royalty-free license, and the agreements under which VLSI acquired the patents-in-suit (and many others) from NXP for $35 million include a provision to share profits ***only if there are any***. Appx4211-4212; Appx14047. VLSI has not shown that NXP is entitled to payment where a license bears no further royalties. The same is true concerning "VLSI's ultimate owners" (VLSI Br. 69)—a collection of sovereign-wealth funds, high-net-worth individuals, pension funds, and other investors who VLSI steadfastly refuses to identify. *VLSI Tech. LLC v. Intel Corp.*, No. 1:18-cv-966-CFC-CJB (D. Del. Aug. 1, 2022), D.I. 975 at 2.

### C. The District Court Improperly Weighed Prejudice.

VLSI does not contest that Intel's license defense would be dispositive or that the district court's finding of no prejudice to Intel was based primarily on its flawed futility analysis. Appx71. The court further erred by finding that amendment would prejudice VLSI because trial had already occurred. *Id.* Intel filed its motion before trial, and the court cannot use its own 16-month delay to find prejudice. Intel Br. 71-72.

## CONCLUSION

The judgment should be reversed or vacated and remanded for a new trial.

Respectfully submitted,

/s/ William F. Lee

AMANDA L. MAJOR
STEVEN J. HORN
WILMER CUTLER PICKERING
HALE AND DORR LLP
1875 Pennsylvania Avenue, NW
Washington, DC 20006
(202) 663-6000

MARY V. SOOTER
WILMER CUTLER PICKERING
HALE AND DORR LLP
1225 17th Street, Suite 2600
Denver, CO 80202
(720) 274-3135

WILLIAM F. LEE
JOSEPH J. MUELLER
LAUREN B. FLETCHER
BENJAMIN N. ERNST
ALISON BURTON
WILMER CUTLER PICKERING
HALE AND DORR LLP
60 State Street
Boston, MA 02109
(617) 526-6000
William.Lee@wilmerhale.com

*Attorneys for Defendant-Appellant Intel Corporation*

January 4, 2023

## CERTIFICATE OF SERVICE

I hereby certify that, on this 4th day of January, 2023, I filed the foregoing Reply Brief for Defendant-Appellant Intel Corporation with the Clerk of the United States Court of Appeals for the Federal Circuit via the CM/ECF system, which will send notice of such filing to all registered CM/ECF users.

/s/ William F. Lee
WILLIAM F. LEE
WILMER CUTLER PICKERING
HALE AND DORR LLP
60 State Street
Boston, MA 02109
(617) 526-6000

**CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS**

The foregoing filing complies with the relevant type-volume limitation of the Federal Rules of Appellate Procedure and Federal Circuit Rules because:

1. The filing has been prepared using a proportionally-spaced typeface and includes 7,000 words.

2. The brief has been prepared using Microsoft Word for Office 365 in 14-point Times New Roman font. As permitted by Fed. R. App. P. 32(g), the undersigned has relied upon the word count feature of this word processing system in preparing this certificate.

/s/ William F. Lee
WILLIAM F. LEE
WILMER CUTLER PICKERING
HALE AND DORR LLP
60 State Street
Boston, MA 02109
(617) 526-6000

January 4, 2023